

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FARID A. YAZDY
and
MICHAEL DHUEY

Appeal No. 1998-1800
Application No. 08/430,453

ON BRIEF

Before RUGGIERO, DIXON, and GROSS, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-10, all of the claims pending in the present application.

The claimed invention relates to a method and apparatus for managing cache memory during cache inhibited transactions. Data stored in the cache memory is updated during write hits

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regardless of whether the address being operated upon is

designated as cache inhibited. Read operations, on the other hand, are performed in a conventional manner in which addresses indicated as noncacheable are not allocated in the cache. Appellants assert at pages 3 and 4 of the specification that this technique permits the cache memory to remain coherent with the main memory even for memory ranges designated as cache inhibited, thereby eliminating the need for flushing the cache when memory areas are redesignated from noncacheable to cacheable.

Claim 1 is illustrative of the invention and reads as follows:

1. A method for managing a cache memory during a memory operation comprising the steps of:

receiving an address at a cache controller;

determining whether said address has been designated as noncacheable;

if said address has been designated as noncacheable and said memory operation is a read operation, then accessing a main memory to retrieve therefrom; and

if said address has been designated as noncacheable and said memory operation is a write operation, then accessing said main memory and updating said cache memory.

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The Examiner relies on the following prior art:

Olson	5,297,270	Mar. 22, 1994
Taylor et al. (Taylor)	5,307,477	Apr. 26, 1994

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Claims 1-10 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner offers Olson alone with respect to claims 1-3, 5, 6, 9, and 10, and adds Taylor to Olson with respect to claims 4, 7, and 8.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs¹ and Answers for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

¹The Appeal Brief was filed May 5, 1997. In response to the Examiner's Answer dated October 28, 1997, a Reply Brief was filed December 29, 1997, which was acknowledged and entered by the Examiner without further comment in the communication dated March 26, 1998.

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It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill

in the art the obviousness of the invention set forth in claims 1-10. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some

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teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

With respect to the appealed independent claims 1-3, 5,

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and 9, the Examiner, as the basis for the obviousness rejection, proposes to modify the disclosure of Olson which provides, during a "split-mode" operation, for updating of cache memory during a read operation even when reading from the cache is inhibited.

The Examiner, while recognizing that Olson does not disclose the updating of cache memory during write operations to noncacheable locations as required by the language of the appealed claims, nevertheless offers the following conclusion (Answer, pages 3 and 4):

In as much as main memory writes will change main memory data, which, if not accounted for, will create a coherency problem if cached data corresponding to the same memory address were not also updated, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have made the device taught by the Olson reference to also update memory writes in the cache while in split mode so that, should a write occur to a non-cacheable location that has been cached, the cache will be up-to-date and therefore be able to immediately supply accurate data as soon as the CPU changes the cacheability status of the given address, as noted to be desirable.

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In response, Appellants assert a lack of establishment by the Examiner of a prima facie case of obviousness. In Appellants' view (Brief, pages 7 and 8; Reply Brief, pages 2-4), not only is Olson completely silent as to the updating of noncacheable locations during write operations, but the skilled artisan, considering the entirety of Olson's disclosure, would be led away from any such write operation updating.

After careful review of the Olson reference in light of the arguments of record, we are in general agreement with Appellants' position as stated in the Briefs. While we do not dispute the correctness of the Examiner's generalized assertion that the quest for accuracy in cache supplied data would extend to write operations as well as read operations, to accept the Examiner's conclusions in the present factual situation, we would have to improperly and selectively ignore significant portions of the Olson disclosure. While it is proper for an Examiner to consider not only the specific teachings of a reference, but also inferences a skilled artisan might draw from them, it is equally important that the

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teachings of prior art references be considered in their
entirety. See In re Preda, 401 F.2d 825,

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826, 159 USPQ 342, 344 (CCPA 1968); W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 1550, 220 USPQ 303, 311 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

In order for us to sustain the Examiner's position we would, at the very least, have to completely divorce Olson's description of the split-mode embodiment illustrated in Figures 4 and 5 from the remainder of the Olson disclosure. Such an approach, however, would be directly contrary to the express disclosure of Olson. Olson describes the Figure 4 split-mode embodiment as a modification of the Figure 1 circuit and, in describing the address decode circuit 43a, discloses that it is identical to the address decode circuit 43 of Figure 1 except for an additional output line to a split-mode control register 97. In our view, the only conclusion that can be drawn from this portion of Olson is that the write operation in the split-mode embodiment, which is never discussed by Olson, must be identical to the write operation specifically described in Figure 3 in relation to the operation of the Figure 1 circuitry. This write operation, illustrated in the right

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branch of the Figure 3 flow diagram, excludes updates to cache memory during writes to noncacheable (i.e., RAM#) locations.

In further support of this interpretation of Olson, we point out, and as also asserted by

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Appellants (Reply Brief, page 6), the left branch of Olson's Figure 5 split-mode flow diagram indicates that reads as well as writes are inhibited (as indicated by the RAM# designation) to noncacheable locations.

In our opinion, since all of the claim limitations are not taught or suggested by the Olson reference, the Examiner has not established a prima facie case of obviousness. Accordingly, we do not sustain the Examiner's 35 U.S.C. § 103 rejection of independent claims 1-3, 5, and 9, nor of claims 6 and 10, dependent thereon.

As to the 35 U.S.C. § 103 rejection of dependent claims 4, 7, and 8 based on the combination of Olson and Taylor, it is apparent from the Examiner's analysis that Taylor was applied solely to address the partial word write limitations of these claims. Taylor, however, does not overcome the innate deficiencies of Olson discussed supra and, therefore, the obviousness rejection of dependent claims 4, 7, and 8 is not sustained.

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In conclusion, we have not sustained the Examiner's rejection of any of the claims on appeal under 35 U.S.C. § 103. Accordingly, the decision of the Examiner rejecting claims 1-10 is reversed.

REVERSED

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JOSEPH F. RUGGIERO)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH L. DIXON)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
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ANITA PELLMAN GROSS)	
Administrative Patent Judge)	

JFR:hh

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