

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KIM C. HARDEE

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Appeal No. 1998-1815  
Application No. 08/684,328

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ON BRIEF

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Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.  
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the rejection of claims 13-46. We reverse.

BACKGROUND

The invention at issue in this appeal is a method for using a sense amplifier in an integrated circuit (IC) memory. An IC memory includes many memory cells, which are arranged in rows and columns. A column is a collection of memory cells

along a bit line pair. Each column is connected to a sense amplifier. The sense amplifier senses the effect a memory cell has on the bit line pair and amplifies a signal for reading data from the memory cell. In addition, the sense amplifier drives, i.e., controls, the bit line pair for writing data into the memory cell.

When conventional sense amplifiers are employed in large memories, the amplifiers work inefficiently and slowly, prolong access time, suffer pattern sensitivities, and are unstable. The invention aims to overcome these problems. In particular, the inventive method includes coupling a local read amplifier in communication with a sense amplifier latch.

Claim 45, which is representative for our purposes, follows:

45. A method of reading data from a first bit line in an integrated circuit memory including the steps of:

operating a sense amplifier latch to develop a first voltage on a first internal latch node communicating with said bit line, said first voltage corresponding to the data on said bit line;

said operating step including operating at least one local sense amplifier drive transistor to provide power to said latch;

coupling said first voltage to a control electrode of a first read amplifier transistor in a local read amplifier communicating with said sense amplifier latch; and

generating a pair of differential signals via said local read amplifier based on said first voltage and the state of said first read amplifier transistor;

wherein said differential signals are generated without disturbing said first internal latch node.

The references relied on in rejecting the claims follow:

U.S. Patent Application 08/674,282 ('282 Application) (filed July 1, 1996)

U.S. Patent Application 08/284,183 ('183 Application) (filed Aug. 2, 1994)

Young 5,247,479 Sep. 21, 1993 (filed May 23, 1991)

Toshiba et al. (Toshiba), European Patent Application 0 175 880 Apr. 2, 1986.

Claims 30-40 and 45-46 stand provisionally rejected under the doctrine of obviousness-type double patenting as unpatentable

over claims 5-7,20-26, and 28-39 of the '282 Application. Claims 43 and 44 stand provisionally rejected under the doctrine of obviousness-type double patenting as unpatentable over claims 8, 9, and 14-50 of the '183 Application. Claims 45 and 46 also stand rejected under 35 U.S.C. § 103 as obvious over Young in view of Toshiba. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

#### OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. Furthermore, we duly considered the arguments of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 13-46. Accordingly, we reverse.

Our opinion addresses the following rejections:

- obviousness-type double patenting
- obviousness.

We begin by addressing the rejections for obviousness-type double patenting.

Obviousness-Type Double Patenting

Regarding the obviousness-type double patenting rejection over claims 5-7, 20-26, and 28-39 of the '282 Application, the appellant argues, "[c]laims 30-40 and 45-46 ... are directed to a method of operating a sense amplifier, i.e. reading, and are not directed to an apparatus which is the subject of the related application." (Appeal Br. at 48.) Regarding the obviousness-type double patenting over claims 8, 9, and 14-50 of the '183 Application, the appellant argues, "[c]laims 43-44 are directed to a method of operating a sense amplifier, i.e. writing, and are not directed to an apparatus, which is the subject of the related application." (Id. at 50.) The examiner collectively responds, "claims-30-40 and 43-46 ... have been amended and changed since the original restriction requirement regardless that the claims are directed to a method, and hence are not consonant with the restriction requirement made by the examiner ...." (Examiner's Answer at 5.)

We note the following principles concerning consonance from Symbol Technologies Inc. v. Opticon Inc., 935 F.2d 1569, 1579, 19 USPQ2d 1241, 1249 (Fed. Cir. 1991).

Consonance requires that the line of demarcation between the "independent and distinct inventions" that prompted the restriction requirement be maintained. Though the claims may be amended, they must not be so amended as to bring them back over the line imposed in the restriction requirement. Where that line is crossed the prohibition of the third sentence of Section 121 does not apply.

Gerber Garment Technology Inc. v. Lectra Systems Inc., 916 F.2d 683, 688, 16 USPQ2d 1436, 1440 (Fed. Cir. 1990). The corollary to this Court's statement in Gerber Garment is that new or amended claims in a divisional application are entitled to the benefit of

§ 121 if the claims do not cross the line of demarcation drawn around the invention elected in the restriction requirement.

With these principles in mind, we address the obviousness-type double patenting rejections over claims 5-7, 20-26, and 28-39 of the '282 Application and over claims 8, 9, and 14-50 of the '183 Application separately.

*Obviousness-Type Double Patenting over the '282 Application*

The examiner fails to show a loss of consonance between claims 5-7, 20-26, and 28-39 of the '282 Application and claims 30-40 and 45-46 of the instant application. In U.S. Patent Application 07/976,312 ('312 Application), the grandparent application of the instant application, the examiner issued a restriction requirement dividing the initial claims into five groups. (Paper No. 3 at 2.) He explained that the second group comprised "[c]laims 5-7, drawn to a sense amplifier utilizing a column read amplifier for read operation" and that the fifth group comprised "[c]laim 13, drawn to a method of operating a sense amplifier utilizing a read amplifier and data write circuitry ...." (Id.) It is uncontested that the appellant elected to prosecute claims 5-7 and claims similar thereto in the '282 Application and its parent application and to prosecute claim 13 and claims similar thereto in the instant application and its parent application. (Appeal Br. at 47.)

Although claims 30-40 and 45-46 have been added to the instant application and amended since the restriction requirement, the examiner fails to allege, let alone show, that the claims have been altered to recite a sense amplifier

utilizing a column read amplifier for read operation or an apparatus of any sort. To the contrary, the claims are still method claims drawn to "[a] method of reading from memory cells associated with corresponding bit lines in an integrated circuit memory . . . ." Because claims 30-40 and 45-46 omit a method, we are not persuaded that the claims cross the line of demarcation drawn in the restriction requirement. Cf. Applied Mats., Inc. v. Advanced Semiconductor Mats., 98 F.3d 1563, 15??, 40 USPQ2d 1481, 1484 (Fed. Cir. 1996) ("In this case consonance was not violated, for the process claims remained in separate patents from the apparatus claims although the scope of the process claims was modified.") Therefore, we reverse the provisional rejection of claims 30-40 and 45-46 over claims 5-7, 20-26, and 28-39 of the '282 Application.

*Obviousness-Type Double Patenting over the '183 Application*

The examiner fails to show a loss of consonance between claims 8, 9, and 14-50 of the '183 Application and claims 43 and 44 of the instant application. In the restriction requirement of the '312 Application, he explained that the

third group comprised "[c]laims 8-9, drawn to a sense amplifier utilizing a data write driver circuit for write operation ...." (Paper No. 3 at 2.) It is uncontested that these are the claims in the '183 Application. (Appeal Br. at 40.)

Although claims 43 and 44 have been added to the instant application and amended since the restriction requirement, the examiner fails to allege, let alone show, that the claims have been altered to recite a sense amplifier utilizing a data write driver circuit for a write operation. To the contrary, the claims are still method claims drawn to "[a] method of writing data to a selected memory cell in an integrated circuit memory having a plurality of sense amplifiers coupled to a plurality of bit lines which are coupled to a plurality of memory cells ...." Because claims 43 and 44 omit a method, we are not persuaded that the claims cross the line of demarcation drawn in the restriction requirement. Therefore, we reverse the provisional rejection of claims 43 and 44 over claims 8,

9, and 14-50 of the '183 Application. We next address the rejection for obviousness.

### Obviousness

We note the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With these principles in mind, we address the examiner's rejection and the appellants' argument.

The examiner's rejection follows in pertinent part. "Young shows all the limitations of the claimed method of reading from memory cells in figs. 1-4, utilizing a sense amplifier latch 21a-24b and a local column read amplifier 28,

25, 27 . . . ." (Final Rejection at 2.) His rejection continues as follows.

Young is applied as stated above.

What is not shown in Young is the use of at least one local sense amplifier drive transistor, as recited in claims 45-46.

However, EP ('880) clearly shows the use of at least one local sense amplifier drive transistor 58 and 61 in figs. 1-13.

In regard to claims 45-46, therefore, to utilize the use [sic] of at least one local sense amplifier drive transistor from the teachings of EP ('880) into Young would have been obvious to one ordinarily skilled in the art to provide the claimed method of reading data because the advantage of the use of at least one local sense amplifier drive transistor is in detail discussed in EP ('880).

(Id. at 4.) The appellant argues, "28,25,27 etc. are not a read amplifier but a column sense amplifier. Likewise, 21a-24b are not a sense amplifier latch but form a memory cell latch." (Appeal Br. at 40.)

Claims 45 and 46 specify in pertinent part the following limitations:

operating a sense amplifier latch to develop a first voltage on a first internal latch node communicating with said bit line, said first voltage corresponding to the data on said bit line;

...

coupling said first voltage to a control  
electrode of a first read amplifier transistor in a  
local read amplifier communicating with said sense  
amplifier latch

....

Accordingly, claims 45 and 46 require coupling a local read  
amplifier in communication with a sense amplifier latch.

The examiner fails to show a suggestion of the  
limitations in the prior art. "Obviousness may not be  
established using hindsight or in view of the teachings or  
suggestions of the inventor." Para-Ordnance Mfg. v. SGS  
Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239  
(Fed. Cir. 1995)(citing W.L. Gore & Assocs., Inc. v. Garlock,  
Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13  
(Fed. Cir. 1983)). "The mere fact that the prior art may be  
modified in the manner suggested by the Examiner does not make  
the modification obvious unless the prior art suggested the  
desirability of the modification."  
In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84  
(Fed. Cir. 1992) (citing In re Gordon, 733 F.2d 900, 902, 221  
USPQ 1125, 1127 (Fed. Cir. 1984)).

The prior art belies the examiner's allegation that elements 21a, 21b, 24a, and 24b of Young form a sense amplifier latch while elements 25, 27, and 28 of the reference form a local column read amplifier. (Final Rejection at 2.) "Every patent application and reference relies to some extent upon knowledge of persons skilled in the art to complement that [which is] disclosed ...." In re Bode, 550 F.2d 656, 660, 193 USPQ 12, 16 (CCPA 1977) (quoting In re Wiggins, 488 F.2d 538, 543, 179 USPQ 421, 424 (CCPA 1973)). Those persons "must be presumed to know something" about the art "apart from what the references disclose." In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962).

Here, U.S. Patent 5,265,047 (Leung) (copy attached), which the examiner "made of record" in the '312 Application, (Paper No. 16 at 5.), evidences that in memory circuits comprising memory cells and a sense amplifier, word lines are used by the memory cells rather than the sense amplifier. Specifically, "two separate word lines (WL and WLC) are used in each memory cell." Col. 3, ll. 54-54. Figure 3 of the reference specifically shows that the word lines WL and WLC

are connected to memory cells 400 and 500 rather than to sense amplifier 504.

Similarly, Figure 2a of Young shows word line WL connected to elements 21a, 21b, 24a, and 24b. As evidenced by Leung and contrary to the examiner's allegation, therefore, persons skilled in the art would interpret the elements as forming a memory latch rather than a sense amplifier latch. Also contrary to the examiner's allegation, such persons would then interpret elements 25, 27, and 28 as the "local or column sense amplifier," col. 1, ll. 65-66, shown in the Figure rather than as a local column read amplifier. In summary, the examiner fails to show that Young teaches a local read amplifier let alone such an amplifier coupled to data read lines and to an internal node of a sense amplifier latch. He fails to allege, let alone show, that Toshiba remedies the defect of Young.

Because Young omits a local read amplifier, we are not persuaded that teachings from the prior art would have suggested the limitations of "operating a sense amplifier

latch to develop a first voltage on a first internal latch node communicating with said bit line, said first voltage corresponding to the data on said bit line; ... coupling said first voltage to a control electrode of a first read amplifier transistor in a local read amplifier communicating with said sense amplifier latch ...."

The examiner fails to establish a prima facie case of obviousness. Therefore, we reverse the rejections of claims 45 and 46 as obvious over Young in view of Toshiba.

CONCLUSION

To summarize, the provisional rejections of claims 30-40 and 45-46 under the doctrine of obviousness-type double patenting as unpatentable over claims 5-7,20-26, and 28-39 of the '282 Application and of claims 43 and 44 under the doctrine of obviousness-type double patenting as unpatentable over claims 8, 9, and 14-50 of the '183 Application are reversed. The rejection of claims 45 and 46 under 35 U.S.C. § 103 as obvious over Young in view of Toshiba is also reversed.

REVERSED

ERROL A. KRASS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
LEE E. BARRETT	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
LANCE LEONARD BARRY	)	
Administrative Patent Judge	)	

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