

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PETER ECCLESINE

Appeal No. 1998-2749
Application 08/637,062¹

ON BRIEF

Before THOMAS, HAIRSTON, and BARRETT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed April 24, 1996, entitled "Network Controller Having Automatically Invoked DMA Data Transfer," which is a division of Application 08/343,073, filed November 21, 1994, now abandoned.

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 12-24 and 26-31. Claim 25 has been allowed.

We affirm-in-part.

BACKGROUND

The disclosed invention is directed to a network controller which allows received data frames to be held in an internal memory buffer and which has the capability to selectively switch between a direct memory access (DMA) mode of data transfer and a non-DMA mode of data transfer to move data frames from the internal memory buffer to a desired location. When an overflow of the memory buffer is anticipated, a DMA controller is automatically engaged to move the data frames from the memory buffer to a system memory to prevent the received frames from being discarded.

Claim 12 is reproduced below.

12. In a network controller for receiving data frames having an internal memory buffer for holding the data frames received from a network for processing by a host processor, and a direct memory access (DMA) circuit transferring received data frames into a system memory, a buffer manager comprising:

a held frame monitor responsive to said memory buffer for monitoring the data frames loaded into said memory buffer and unloaded from said memory buffer, and

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decision logic responsive to said held frame monitor for automatically engaging said DMA circuit to unload the data frames from said memory buffer when overflow of said memory buffer is anticipated.

The Examiner relies on the following prior art:

Petersen et al. (Petersen)	5,307,459	April 26, 1994
Hausman et al. (Hausman)	5,412,782	May 2, 1995 (filed July 2, 1992)
Gunji	5,487,154	January 23, 1996 (filed July 14, 1992)

Claims 12-14, 19, 20, and 26-31 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hausman.

Claims 15-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hausman and Petersen.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hausman.

Claims 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hausman and Gunji.

We refer to the first Office action (Paper No. 2), the final rejection (Paper No. 4), and the examiner's answer (Paper No. 9) (pages referred to as "EA__") for a statement of the Examiner's position, and to the appeal brief (Paper No. 8) (pages referred to as "Br__") for a statement of Appellant's arguments thereagainst.

OPINION

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Claims 12-14, 19, 20, and 26-31

As to claims 12, 19, 26, and 27, Appellant argues that the field RX Bytes in Hausman measures the number of bytes stored in the buffer and has nothing to do with the frame count (Br6). The Examiner responds that claim 12 does not expressly recite counting frames, and the held frame monitor could count the number of data words (EA6). The Examiner points to page 20 of the specification, which describes that the threshold value could be based on the capacity of the memory buffer (EA6).

We agree with the Examiner that "a held frame monitor . . . for monitoring the data frames loaded into said memory buffer and unloaded from said memory buffer" does not positively require keeping a frame count, i.e., "monitoring the data frames" is not "monitoring the number of data frames." The limitation of "monitoring the data frames" can be broadly interpreted to read on keeping track of the buffer capacity as shown in the RX Bytes field in Hausman. This interpretation is consistent with Appellant's specification which describes that the threshold value can be based on the number of data frames or the number of data words loaded into the buffer (specification, p. 20, lines 3-28). A "packet" is defined as "[s]ynonymous with data frame," IBM

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Dictionary of Computing (McGraw-Hill, Inc., 10th ed., 1993) (copy attached). Thus, the packets in Hausman are "data frames" as claimed. Since Hausman deals with packets of variable length, Hausman keeps track of bytes rather than a number of fixed length data frames. Claim 12 does not recite fixed length data frames and such an implied limitation is not read into the claim. For these reasons, we sustain the rejection of claims 12, 19, 26, and 27.

Appellant argues that the Examiner has not identified where Hausman teaches the loader limitation of claim 13 and the unloader limitation of claim 14 (Br6). We interpret this as an argument that Hausman does not teach these limitations since it would be misleading to argue that the Examiner has not shown where the limitations are found if Appellant knew that the limitations were, in fact, disclosed. The Examiner finds, as to claim 13, that DMA ring buffer Write index specifies the address to which the next byte will be written (EA6) and, as to claim 14, the DMA ring buffer Read index specifies the address of the next byte to be read (EA7).

Although we find that the Examiner errs in relying on the DMA ring buffer, we find the limitations of claims 13 and 14 to be

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inherent in Hausman. The DMA ring buffer is contained in the host memory, which is a different memory from the RX FIFO 170 which the Examiner relies on as the claimed "buffer memory" in claim 12. Thus, indices for writing and reading into the DMA Ring Buffer are not relevant to claims 13 and 14. However, the RX RAM FIFO 170 is a random access memory (RAM) first-in first-out (FIFO) buffer. It was notoriously well known to those of ordinary skill in the computer art that RAM FIFOs have means to generate storage addresses for writing and reading data in a first-in first-out order; i.e., new data is written to the logical bottom of the buffer and the oldest data is read from the logical top of the buffer with indices (pointers) to keep track of the addresses of the top and bottom data values (like the DMA ring buffer Write index and Read index). Hausman discloses (col. 8, lines 19-23): "If DMA mode is initiated, the DMA controller will begin copying bytes from the top of RX FIFO 170 into the DMA ring buffer, while receive circuitry 130 may be continuing to add data to the bottom of RX FIFO 170." Manifestly, Hausman inherently must have means for determining the addresses of the top and bottom of the FIFO buffer for reading and writing, respectively. For these reasons, we sustain the rejection of claims 13 and 14.

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With respect to claim 20, Appellant argues (Br6) that the Examiner has not identified what corresponds to the "decision logic" which compares the count value of the held frame counter "with a variable threshold value to determine whether to engage said DMA circuit in unloading said memory buffer" (emphasis added). The Examiner finds that Hausman teaches (at col. 3, lines 10-42) an adapter programmed to initiate DMA backup mode once receive FIFO 170 has less than a receive FIFO free byte threshold number of remaining available bytes (EA7).

The Examiner does not address the "variable" limitation. As disclosed by Appellant, the variable threshold value "may be based on the rate of unloading said data frames from the memory buffer" (specification, p. 8, lines 10-12; claim 21). Hausman discloses a fixed FIFO free byte threshold number indicating the remaining available bytes in the RX FIFO 170 (col. 3, lines 33-42; figure 5, step 520), i.e., a fixed DMA enable threshold. While Hausman discloses an adjustable (variable) Early Receive (Early RX) Threshold, this has to do with the data transmission, not a DMA backup mode (col. 3, lines 10-32). Thus, we find that Hausman does not describe a "variable threshold value." The rejection of claim 20 is reversed.

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With respect to claim 28, Appellant argues that the Examiner has made no showing that any of the references adds status and length fields at the beginning of a frame when the frame is completely loaded (Br7). The Examiner states that it is inherent that the status and length fields are added at the beginning of a frame when the frame is completely loaded, referring to column 4, lines 5-19 (EA7).

We fail to see how Hausman inherently discloses adding status and length fields at the beginning of a frame when the frame is completely loaded. Figure 3B, to which the Examiner refers, deals with the format of a receive packet 320. Although the receive packet 320 has status and length fields, these are part of the packet as received and are not added when the frame (packet) is completely loaded and are not added to the beginning of the frame. Accordingly, we find that claim 28 is not anticipated. The rejection of claim 28 is reversed.

Appellant argues that, with respect to claim 29, the Examiner has not shown a DMA circuit in which DMA access logic is provided on chip and the DMA controller is provided off chip and, with respect to claim 30, the Examiner has not shown an architecture in which the internal buffer memory is provided on chip (Br7). The

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Examiner finds that Hausman teaches DMA control circuitry on an Application Specific Integrated Circuit (ASIC) and a DMA controller which is off chip to issue commands to control the adapter 10 which contains the DMA control circuit (EA8).

Hausman discloses that DMA circuitry is contained within host interface 200 (col. 8, lines 10-11), which is within the ASIC chip, and then refers to the DMA controller (col. 8, lines 19 and 23), implying that the DMA controller is part of the DMA circuitry on the ASIC chip and not off chip. While the host DMA ring buffer is off chip in the host memory (col. 8, lines 6-10), this is not a DMA controller. Claim 29 is not anticipated because it does not teach locating the DMA controller external to the chip. While the decision as to whether to locate functional components, such as the DMA controller, on or off a chip may be within the level of ordinary skill in the art, the rejection here is based on anticipation, not obviousness. Accordingly, the rejection of claim 29 is reversed. Hausman expressly discloses the internal buffer, RX RAM FIFO 170, provided on the ASIC as recited in claim 30; however, because claim 30 depends on claim 29, the rejection of claim 30, and its dependent claim 31, is reversed.

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Claims 15-18

The Examiner finds that Hausman does not explicitly teach generating addresses to allow the host processor to read data frames from the memory buffer, but finds Petersen teaches using host interface logic for transferring data between the host system memory and adapter memory, referring to Host Interface Logic 102, figure 5 (Paper No. 2, p. 5). The Examiner concludes with respect to claim 15 (Paper No. 2, pp. 5-6):

It would have been obvious . . . to combine the teachings of Hausman to provide Petersen's Host Interface Logic for generating addresses to allow data transfer between said host system memory and said memory buffer because it would reduce host processor interrupt latency.

Appellant argues that the addressing scheme in Petersen has nothing to do with reducing processor interrupt latency and, thus, the Examiner's rationale is not appropriate (Br7-8).

We are not persuaded by the Examiner's reasoning using Petersen. While Petersen discloses a host interface logic 102 which is responsive to accesses across the host bus to operate to transfer data between the specified block of addresses 101 in the host memory space and the independent memory (col. 12, lines 22-32), we fail to see how this suggests modifying Hausman to arrive at the claimed subject matter of claim 15. Accordingly,

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we conclude that the Examiner has failed to establish a prima facie case of obviousness with respect to claim 15. The rejection of claim 15, and its dependent claims 16-18, is reversed.

There is a potential question whether the limitations of claims 15-18 are inherent in Hausman. The data transfer operation between the adapter 10 and the host processor in Hausman (non-DMA mode) is normally performed by programmed I/O (PIO) and, so, it seems there inherently must be structure within blocks 160, 180, and 200 that generates addresses to allow the host to read data frames as recited in claim 15. Further, since Hausman loads (writes) data into buffer 170, unloads (reads) data during a DMA mode, and reads data during a host PIO mode, and since memories can only write information from a single source or read information to a single destination at one time, it seems that Hausman inherently must have a multiplexer and memory arbitrator to read/write during these three modes as recited in claims 16-18. However, the rejection is not based on inherency and, in the absence of evidence, we decline to raise a new ground of rejection.

Claim 21

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Although we reversed the anticipation rejection of claim 20, from which claim 21 depends, we address the obviousness rejection of claim 21 in case it cures the deficiencies in the rejection of claim 20.

The Examiner found, with respect to claim 20, that Hausman teaches a variable threshold value which is varied in accordance with the rate of loading of data frames into the memory buffer. The Examiner concludes, with respect to claim 21, that "[i]t would have been [an] obvious matter of design choice to one of ordinary skill in the Data Processing art at the time of the invention to use rate of unloading data frames because it would perform equally well [as using the rate of loading]" (Paper No. 2, p. 6).

Claim 20 recites a variable threshold value to determine whether to engage the DMA circuit in unloading the memory buffer, not just any variable threshold. The threshold to which the Examiner refers is an adjustable (variable) Early Receive (Early RX) Threshold, which has to do with the data transmission, not with the DMA backup mode (col. 3, lines 10-32). For this reason, we reversed the anticipation rejection of claim 20. Since Hausman does not disclose a variable DMA threshold, it does not suggest a variable threshold based on the rate of unloading of

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data frames from the buffer memory. The rejection of claim 21 is reversed.

Claims 22-24

The Examiner finds that Hausman does not explicitly teach a timer, but finds that the abstract of Gunji teaches data reception and transmission are performed through a DMA if the digital signal processor cannot process data fast enough to prevent data loss (Paper No. 2, p. 7). The Examiner concludes (Paper No. 2, p. 7): "It would have been obvious . . . to combine the teachings of Gunji and Hausman to use DMA data transfer mode when data frames are not being processed by a predetermined period because it would prevent data being lost."

Appellant argues that "neither Hausman et al. nor Gunji talk about initiating data transfer in response to expiration of 'a predetermined period of time'" (Br10).

Appellant's argument refers to the limitations of claim 24, not parent claims 22 and 23. Since the limitations of claims 22 and 23 are not argued, we sustain the rejection of claims 22 and 23 pro forma. As to claim 24, Gunji discloses enabling a DMA transfer mode when the signal processing period (T_{cal}) of the digital signal processor (DSP) 2 is greater than the I/O period

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(T_{i0}) of the A/D converter (col. 4, lines 47-61). This does not suggest unloading based on a time interval during which frames are loaded into a buffer memory. Thus, the Examiner has failed to establish a prima facie case of obviousness with respect to claim 24. The rejection of claim 24 is reversed.

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CONCLUSION

The rejections of claims 12-14, 19, 22, 23, 26, and 27 are sustained.

The rejections of claims 15-18, 20, 21, 24, and 28-31 are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
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