

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 34

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROSHI KANEKURA

Appeal No. 1999-0485
Application 08/526,781

ON BRIEF

Before BARRETT, FLEMING, and LALL, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 3, 6, 11, 13 through 16, 18 through 20, and 22 through 28, all of the claims pending in the present application. Claims 2, 4, 5, 7 through 10, 12, 17, and 21

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have been canceled.

The invention relates to operation apparatus that can be used in general-purpose microcomputers or the like, and more particularly, to improvement of an operation apparatus for digital signal processing.

Independent claim 1 is reproduced as follows:

1. An operation apparatus for carrying out an instruction specifying a combined operation of an arithmetic operation and a shifting operation using digital data of n bit length, comprising:

instruction decoding means for decoding the instruction into an arithmetic instruction indicative of the arithmetic operation of the instruction and a shifting instruction indicative of the shifting operation of the instruction;

arithmetic operation means, coupled to said instruction decoder means, for receiving said digital data, carrying out one of a plurality of arithmetic and logical operations according to the arithmetic instruction in response to said digital data, and providing an operation resultant data of $2n$ bit length over one of a plurality of outputs in which at least precision of said combined operation is guaranteed;

selection means, coupled to said arithmetic operation means, for selecting the one of the plurality of outputs on which said operation resultant data is provided in accordance with a selection signal provided by said instruction decoding means;

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shifting operation means having $2n$ bit width capacity, operatively coupled to said selection means to receive said selected operation resultant data, for carrying out a shifting operation in response to said selected operation resultant data according to the shifting instruction; and

rounding processing means, coupled to receive an output value of said shifting operation means, for rounding the output value of said shifting operation means to n -bit length in accordance with a rounding instruction provided by said instruction decoding means, said rounding processing means not rounding the output value of said shifting operation means when the arithmetic instruction is indicative of a logical operation and rounding the output value of said shifting operation means when the arithmetic instruction is indicative of an arithmetic operation,

said combined operation specified by the instruction being performed during a single instruction execution period.

The Examiner relies on the following reference:

Toriumi et al. (Toriumi)	5,260,897	Nov.
9, 1993		

Claims 1, 3, 6, 11, 13 through 16, 18 through 20, and 22 through 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Toriumi.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs¹ and the answer for

¹Appellant filed an appeal brief on February 19, 1998. Appellant filed a reply brief on July 10, 1998. The Examiner mailed an office communication on July 16, 1998 stating that the reply brief has been considered and entered.

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the respective details thereof.

OPINION

We will not sustain the rejection of claims 1, 3, 6, 11, 13 through 16, 18 through 20, and 22 through 28 under 35 U.S.C. § 103.

The Examiner has failed to set forth a **prima facie** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. **In re Sernaker**, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." **Para-Ordnance Mfg. V. SGS Importers Int'l, Inc.**, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), **citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.**, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983).

On page 9 of the brief, Appellant argues that the rounding processing means of claim 1 selectively rounds the $2n$ bit with output from the shifting operation means to n bit length in accordance with the rounding instruction provided by the instruction decoding means. Appellant respectfully submits that Toriumi does not disclose or even remotely suggest these features.

On page 20 of the brief, Appellant argues that claim 6 recites an arithmetic means as providing operation resultant data of $2n$ bit length over one of the plurality of outputs. The selection means selects one of the plurality of outputs on which the operation resultant data is provided in accordance with a selection signal provided by the instruction means. The shifting operation means is recited as having $2n$ bit width capacity. The rounding processing means rounds an output of the shifting operation means to n -bit length in accordance with the rounding signal provided by the instruction means. The rounding processing means is further recited as not

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rounding the output of the shifting operation means when the arithmetic instruction is indicative of a logical operation and rounding the output of the shifting operation when the arithmetic instruction is indicative of an arithmetic operation. Appellant respectively submits that Toriumi does not disclose or suggest these limitations as recited in Appellant's claim 6.

On pages 22 and 23 of the brief, Appellant argues that claim 13 recites an apparatus for performing a combined processing operation on a received data packet which includes digital data and instruction data. The apparatus is recited as including a combination, an instruction decoder, an arithmetic operator, a shifter and a rounding unit. The rounding unit is recited as rounding the shift data when the arithmetic operator provides resultant data based on an arithmetic operation and not for rounding the shift data when the arithmetic operator provides resultant data based on a logical operation. Appellant argues that Toriumi does not disclose these limitations as recited in Appellant's claim 13.

On page 24 of the brief, Appellant argues that

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Appellant's claim 25 is directed to a method of performing a combined processing operation on a received data packet which includes digital data and instruction data and includes in combination steps a) through d). Appellant points out that step d) as claimed includes rounding the shift data when the resultant data is provided based on an arithmetic operation and not rounding the shift data when the resultant data is provided based on a logical operation. Appellant argues that Toriumi does not disclose these limitations as recited in Appellant's claim 25.

We note that Appellant's claim 1 recites

rounding processing means, coupled to receive an output value of said shifting operation means, for rounding the output value of said shifting operation means to n-bit length in accordance with a rounding instruction provided by said instruction decoding means, said rounding processing means not rounding the output value of said shifting operation means when the arithmetic instruction is

indicative of a logical operation and rounding the output value of said shifting operation means when the arithmetic instruction is indicative of an arithmetic operation.

We further note that Appellant's claim 6 recites

rounding processing means, coupled to said shifting operation means, for rounding an output of said shifting

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operation means to n-bit length in accordance with a rounding signal provided by said instruction means, said rounding processing means not rounding the output of said shifting operation means when the arithmetic instruction is indicative of a logical operation and rounding the output of said shifting operation means when the arithmetic instruction is indicative of an arithmetic operation.

We note that Appellant's claim 13 recites

a rounding unit, coupled to said shifter, for rounding the shift data when said arithmetic operator provides resultant data based on an arithmetic operation and for not rounding the shift data when said arithmetic operator provides resultant data based on a logical operation.

Finally, we note that Appellant's claim 25 recites method step

d) rounding the shift data when the resultant data is provided based on an arithmetic operation and not rounding the shift data when the resultant data is provided based on a logical operation.

Thus, we find that all the independent claims require a rounding process which selectively rounds based on an arithmetic operation or selectively does not round based upon a logical operation.

On pages 4 and 5 of the answer, the Examiner acknowledges

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that Toriumi does not teach a rounding processing means that rounds the output of the shifting operation means when the instruction is indicative of an arithmetic operation and does not round the output of the shifting operation means when the instruction is indicative of a logical operation. In response to the Appellant's argument, the Examiner on page 7 of the answer agrees that Toriumi fails to disclose a rounding processing means as claimed but argues that one of ordinary skill in the art would be motivated to provide such a rounding means as claimed. The Examiner cannot provide or point to any indication in Toriumi that provides support for this assertion.

Upon our review of Toriumi, we fail to find that Toriumi teaches or suggests a rounding processing means or a rounding step as recited in Appellant's claims. We note that it is the burden of the Examiner to provide such evidence.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires

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this evidence in order to establish a **prima facie** case. **In re Piasecki**, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984); **In re Knapp-Monarch Co.**, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); **In re Cofer**, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Furthermore, our reviewing court states in **In re Piasecki**, 745 F.2d at 1472, 223 USPQ at, 788 the following:

The Supreme Court in **Graham v. John Deere Co.**, 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under section 103. As adapted to **ex parte** procedure, **Graham** is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103." (**Citing In re Warner**, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)).

On page 7 of the answer, Appellant refers to reference Cocanougher, U.S. Patent No. 5,212,662. We note that this reference was not relied upon in the rejection. Our reviewing court has stated that where a reference is relied on to support a rejection, whether or not in a minor capacity, there would appear to be no excuse for not positively including the reference in the statement of the rejection. **In re Hoch**, 428 F.2d 1341, 1342, 166 USPQ 406, 407 (CCPA 1970).

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In view of the foregoing, we have not sustained the rejection claims 1, 3, 6, 11, 13 through 16, 18 through 20, and 22 through 28 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

LEE E. BARRETT)
Administrative Patent Judge)
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) BOARD OF PATENT
MICHAEL R. FLEMING)
Administrative Patent Judge) APPEALS AND
)
) INTERFERENCES
)
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