

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte HIROSHI KANNO

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Appeal No. 1999-1630  
Application No. 08/784,775

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ON BRIEF

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Before KRASS, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-6, all of the pending claims.

The invention is directed to a level conversion circuit that converts an ECL level or current mode

logic (CML) level signal to a MOS level signal. This is said to permit a level conversion circuit which operates at high speed even at a low power-supply voltage.

Representative independent claim 1 is reproduced as follows:

1. A level conversion circuit comprising:

a first bipolar transistor having a base supplied with a first reference voltage;

a first resistor having a first end connected to a first potential line and a second end connected to the emitter of said first bipolar transistor;

a second resistor having a first end connected to a second potential line and a second end;

a third resistor having a first end connected to said second potential line and a second end;

a first MOS transistor of a first channel type having a gate coupled to an input terminal, a source coupled to the collector of said first bipolar transistor and a drain coupled to the second end of said second resistor;

a second MOS transistor of said first channel type having a gate supplied with a second reference voltage, a source coupled to the collector of said first bipolar transistor and a drain coupled to the second end of said third resistor;

a third MOS transistor of a second channel type having a gate directly connected to the drain of said first MOS transistor, a source coupled to said second potential line and a drain;

a fourth MOS transistor of said second channel type having a gate directly connected to the drain of said second MOS transistor, a source coupled to said second potential line and a drain;

a fifth MOS transistor of said first channel type having a gate coupled to the drain of said fourth MOS transistor, a drain coupled to the drain of said fourth MOS transistor and a source coupled to a third potential line;

a sixth MOS transistor of said first channel type having a gate coupled to the gate of said fifth



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Appellant does not dispute the examiner's characterization of APA and agrees that the difference between the instant claimed invention and APA is in the former's use of MOS transistors for APA's bipolar transistors Q2-Q3. It is appellant's position, and the reason for the instant invention, that the use of bipolar transistors Q2-Q3 suffer from the problem that the outputs of the amplitude amplification section have to be sufficiently low in order to completely turn on one transistor of the P-channel MOS transistors P1 and P2 of the input section of the level conversion section and completely turn off the other transistor. Otherwise, either the level conversion section would be inoperable or the operating speed would become slow. On the other hand, if the low level of the amplitude amplification section output is set to a sufficiently low value such that its highest value is still low enough, there will be a problem that the collector potentials of the NPN transistors Q2 and Q3, which constitute the current switches of the amplitude amplification section, will be overreduced and the transistors will be saturated and the operating speed will be reduced, when the low level of the output fluctuates conversely in the lowest direction.

Appellant allegedly solves these problems by providing a pair of MOS transistors of a first channel type (claim 1), and providing a pair of N-channel MOS transistors (claim 3).

While Nagasawa may show two MOS transistors as claimed, in order for a proper rejection under 35 U.S.C. 103 to lie, there must be some reason for the artisan to have modified APA by replacing the two bipolar transistors with the MOS transistors of Nagasawa. The artisan must have been led to

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make such a modification by some teaching or suggestion in the prior art or by some knowledge possessed by the theoretical artisan skilled in the art.

The examiner contends that this reason is provided by Nagasawa's teaching of reducing power consumption and the artisan's desire to reduce power consumption in APA. While that may be a sufficient reason to make a modification, the examiner has not convinced us that Nagasawa's use of MOS transistors Q1-Q2 is what provides the power consumption reduction in Nagasawa.

It is appellant's contention that Nagasawa does not use MOS transistors Q1-Q2 for the purpose of reducing power consumption as suggested by the examiner. Instead, appellant suggests, Nagasawa's reduced power consumption is achieved by restraining the voltage applied to the constant current source. We agree with appellant that column 4, lines 6-9, of Nagasawa provides for a voltage applied to the constant current source to be restrained, "thereby reducing current consumption." Since the constant current sources are "designated by combinations Q5-Q7 resistors R1-R3" [column 2, lines 33-35, of Nagasawa], any part played by MOS transistors Q1-Q2 in reducing power consumption is indirect and these transistors would need to be brought to APA along with other elements in order to achieve the power consumption reduction achieved by Nagasawa. The examiner cannot bring only so much of the prior art as is needed in order to construct the instant claimed subject matter, while leaving other important elements of the prior art which work in tandem with the elements the examiner is extracting. It would appear the only reason for doing so is hindsight gained from knowledge of

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appellant's own disclosure since neither APA nor Nagasawa suggests the modification being made by the examiner. This, of course, is an improper basis for reaching the conclusion of obviousness of the instant claimed subject matter.

The examiner contends that it is "old and well known" in the art to employ MOS transistors for their superiority over bipolar transistors in achieving power consumption reduction [answer-page 4]. However, even if we adopt the examiner's position that MOS transistors should be substituted for bipolar transistors because of their alleged "superiority," why is the examiner contending that it would have been obvious to replace APA's transistors Q2-Q3 with MOS transistors but no mention is made of replacing APA's bipolar transistor Q4? If MOS transistors are "superior," why not just replace all bipolar transistors of APA with MOS transistors? Again, it appears that the examiner is merely picking and choosing only so much of the prior art that is necessary to meet the instant claimed limitations without regard to the interaction between other circuit elements.

Accordingly, we will not sustain the rejection of claims 1-6 under 35 U.S.C. 103 because, in our view, the examiner has not set forth a prima facie case of obviousness. We do not mean to imply that, perhaps, a prima facie case could not have been made; only that the examiner has not done so.

We also do not agree with appellant's argument [reply brief-page 2] that the examiner's rationale was flawed because the present invention was designed to solve the problem of saturation of the collector potentials of the bipolar transistors Q2 and Q3 of APA which results in reduced operating

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speed, while the examiner contends that reduced power consumption is a reason that would have led the artisan to make modifications to APA. If the claimed subject matter results from a suggestion by the prior art to make a modification, albeit for different reasons than those of an applicant, a proper rejection may, nevertheless, lie under 35 U.S.C. 103. Our decision herein results, not because reduced power consumption was employed for the reason for modification, but because, in our view, the examiner's reason for modifying APA by changing the bipolar transistors of APA to the MOS transistors of Nagasawa (i.e., for reduced power consumption) was not consistent with the disclosure of Nagasawa with regard to the elements actually causing the reduction in power consumption.

The examiner's decision is reversed.

REVERSED

ERROL A. KRASS	)
Administrative Patent Judge	)
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	) BOARD OF PATENT
JOSEPH F. RUGGIERO	) APPEALS AND
Administrative Patent Judge	) INTERFERENCES
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HOWARD B. BLANKENSHIP     )  
Administrative Patent Judge    )

EK/RWK

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