The opinion in support of the decision being entered today was **not** written
for publication and is **not** binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RON-FU CHU, YANG PAN, QUN YING LIN
and MEI SHENG ZHOU

Appeal No. 1999-1872
Application No. 08/657,219

ON BRIEF

Before KIMLIN, PAK, and LIEBERMAN, Administrative Patent Judges.

LIEBERMAN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the decision of the examiner refusing to allow claims 1 through 4, 6 through 8, 10, 12 through 15 and 17, as amended subsequent to the Final Rejection, which are all of the claims pending in this application.

THE INVENTION

The invention is directed to a method of forming a polysilicon gate electrode wherein the surface of the polysilicon is roughened to a depth of less than 50 Angstrom units. Following etching of the polysilicon layer, a polysilicon gate electrode is formed wherein the gate electrode has a roughened polysilicon surface. Roughening the polysilicon surface typically occurs using a plasma etching process. Additional limitations are disclosed in the following illustrative claim.

THE CLAIM

Claim 1 is illustrative of appellants' invention and is reproduced below.

1. A method of forming a polysilicon gate electrode in the fabrication of an integrated circuit device comprising:

providing bare active areas surrounded by field oxide isolation on a semiconductor substrate wherein the surface of said substrate has an uneven topography due to the uneven interface between said active areas and said isolation;

depositing a polysilicon layer over said active areas and said field oxide isolation of said substrate;

roughening the surface of said polysilicon layer to a depth of less than 50 Angstroms;

covering said roughened polysilicon layer with a layer of photoresist;

exposing portions of said photoresist layer not covered by a mask to actinic light wherein other portions of said photoresist layer covered by said mask are unexposed;

developing and patterning said photoresist layer to form the desired photoresist mask for said polysilicon layer; and

etching away said polysilicon layer where it is not covered by said photoresist mask to form said polysilicon gate electrode wherein said polysilicon gate electrode has a roughened polysilicon surface in the fabrication of said integrated circuit device.

THE REFERENCES OF RECORD

As evidence of obviousness, the examiner relies upon the following references:

Tsou	5,007,982	Apr. 16, 1991
Hur	5,670,298	Sep. 23, 1997 (filed Jan. 11, 1996)

THE REJECTION

Claims 1 through 4, 6 through 8, 10, 12 through 15 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicants' admission in view of Hur and Tsou.

OPINION

We have carefully considered all of the arguments advanced by the appellants and the examiner and agree with the appellants that the rejection of claims 1 through 4, 6

through 8, 10, 12 through 15 and 17 are not well founded.[1] Accordingly, we reverse this rejection.

The Rejections under § 103(a)

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The examiner relies upon a combination of two references and appellants' admission to reject the claimed subject matter and establish a prima facie case of obviousness. It is the examiner's position that, "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conventional method of forming a polysilicon gate electrode in the fabrication of an integrated circuit device to eliminate the use of ARCs, and instead roughen the polysilicon layer to reduce reflectivity and thus notch formation in the mask, motivated by the desire to save money, process steps, lower difficulty of manufacture and further eliminate notch formation in the photoresist mask." See Answer, pages 5 and 6. We disagree.

The admitted prior art relied upon by the examiner is discussed in the specification on page 1 and 2, and is directed to Figures 1 through 3. The aforesaid discussion is directed to the formation of "a partially completed integrated circuit." The appellants state

[1]We refer to the Brief received Nov. 30, 1998.

that, "[w]hen the photoresist is exposed to actinic light, light waves 18 will reflect off the polysilicon surface onto the unexposed portion of the photoresist 20. After the photoresist is developed, as shown in Fig. 2, notches 22 will be found in the resulting photomask. These notches 22 are caused by directional reflection lights." See specification, page 1.

In a further description of the prior art the appellants state that, "[a]nti-reflection coatings (ARC) have been used in semiconductor manufacturing to suppress reflection lights during the masking process. The use of the ARC's allows for the definition of sharp images and the avoidance of resist notching. However, these additional ARC layers are expensive, require additional processing steps, and difficult to control, in manufacturing." See specification, page 2.

In the rejection of record, the prior art discussed in Hur likewise discloses the conventional method of utilizing ARC's. See Hur column 2, line 13 to 67. See also Answer, page 4. We find that Hur eliminates the need for ARC films. See column 2, line 55 to column 3, line 8. We find that Hur replaces the Arc films with a porous film. Id. Figure 3a of Hur discloses that, "a metal film 32 is formed on a semiconductor substrate 31 using a CVD method and then a porous film 33 such as O_3/TEOS oxide film is coated on the metal film 32 under a low temperature." See column 3, lines 41-44.

"Subsequently a photoresist film 34 is formed on the porous film 33, as shown in FIG. 3b and then the photoresist film 34 is subjected to a photolithography process using a

mask having a pattern, thereby forming a photoresist pattern 34-1 shown in Fig. 3c." See column 3, lines 45-49. Thereafter, "the metal film 32 and the porous film 33 are patterned using the remaining photoresist pattern 34-1 as an etch mask. The remaining porous film 33 is then removed to form a desired metal pattern film." See column 3, lines 51 to column 4, lines 3. As stated by the examiner Hur doses not disclose polysilicon. See Answer, page 4.

Finally, the examiner relies on Tsou for its disclosure that, "plasma has long been used to etch or roughen polysilicon " See Answer, page 5.

The process of the claimed subject matter requires, "roughening the surface of said polysilicon layer to a depth of less than 50 Angstroms," a limitation not disclosed by the references of record. Moreover, the claimed subject matter requires formation of a product wherein "said polysilicon gate electrode has a roughened polysilicon surface in the fabrication of said integrated circuit device." See claim 1. The record before us is predicated on the substitution of polysilicon for the porous film of Hur. However, as stated by Hur, the entire porous film is then removed to form a desired metal pattern film. See column 4, lines 1-2. Accordingly, even were one to replace the porous film of Hur with a polysilicon, one would still not obtain the invention of the claimed subject matter. In addition, there is no evidence in the record that teaches or suggests that polysilicon is a porous film within the scope of Tsur.

Based upon the above considerations, even if the examiner was correct in combining the admitted prior art with Hur and Tsou in the manner described in the Answer, the omission of the above-mentioned requisite method limitations with regard to roughening the surface of polysilicon during process formation and having a roughened polysilicon surface present in the polysilicon gateway electrode, as required by the claimed subject matter, would result in a method and product created that would, in any event, fall short of the invention defined by the claimed subject matter, as the aforesaid claimed subject matter requires features that cannot be achieved by combining the references. **Uniroyal,** Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988). Accordingly, the examiner has not established a prima facie case of obviousness.

Furthermore, based on the record before us, the fact that polysilicon in and of itself may be etched and roughened does not provide the requisite motivation to substitute polysilicon for the porous films of Hur. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("[T]he best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.").

DECISION

The rejection of claims 1 through 4, 6 through 8, 10, 12 through 15 and 17 under 35 U.S.C. § 103(a) as being unpatentable over applicants' admission in view of Hur and Tsou is reversed.

The decision of the examiner is reversed.

REVERSED

EDWARD C. KIMLIN Administrative Patent Judge	)	
CHUNG K. PAK Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PAUL LIEBERMAN Administrative Patent Judge	)	

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JUDGE LIEBERMAN

APPEAL NO. 1999-1872

APPLICATION NO. 08/657,219

APJ LIEBERMAN

APJ PAK

APJ KIMLIN

DECISION: **REVERSED**

PREPARED: Nov 19, 2002

OB/HD

PALM

ACTS 2

DISK (FOIA)

REPORT

BOOK