The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY P. GAMBINO
and WILLIAM F. LANDERS

Appeal No. 1999-2115
Application No. 08/724,574

ON BRIEF

Before KIMLIN, LIEBERMAN, and DELMENDO, Administrative Patent Judges.

DELMENDO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the examiner's refusal to allow claims 1 through 20 as amended subsequent to final rejection. These are all of the claims pending in the above-identified application.

The subject matter on appeal relates to a method for removing scratches from a dielectric layer (claims 1-8), a method for manufacturing an integrated circuit chip (claims 9-

14), and an integrated circuit chip (claims 15-20). In particular, the scratches formed during a chemical mechanical polish (CMP) process are removed by heating the dielectric layer to a temperature high enough to cause the dielectric layer to reflow, thereby filling in the scratches and providing a smooth, planar surface for subsequent processing steps. (Appeal brief, page 2.) Further details of this appealed subject matter are recited in illustrative claims 1 and 9, the sole independent claims on appeal:

> 1. A method for removing scratches from a dielectric layer comprising the steps of:
> providing a layer of a reflowable dielectric material;
> subjecting the layer to a chemical mechanical polish; and
> removing scratches formed during the chemical mechanical polish by heating the layer of the reflowable dielectric material to a temperature sufficient to cause the reflowable dielectric material to reflow.
>
> 9. A method for manufacturing an integrated circuit chip comprising the steps of:
> providing a substrate;
> depositing a layer of a reflowable dielectric material on a surface of the substrate;
> defining a pattern in the layer of the reflowable dielectric material, thereby forming a patterned substrate;
> non-selectively depositing a conductive layer over a surface of the patterned substrate;
> chemical mechanical polishing the conductive layer to the surface of the patterned substrate; and

removing scratches on the surface of the dielectric material by heating the layer of the reflowable dielectric material to a temperature sufficient to cause the reflowable dielectric material to reflow.

The examiner relies on the following prior art references as evidence of unpatentability:

Morimoto	4,721,548	Jan. 26, 1988
Rao et al. (Rao)	4,799,992	Jan. 24, 1989
Tang	5,198,387	Mar. 30, 1993
Yu et al. (Yu '534)	5,244,534	Sep. 14, 1993
Yu et al. (Yu '843)	5,314,843	May 24, 1994

The following grounds of rejections are presented for our review in this appeal:

I. Claims 1 through 4, 6, and 8 under 35 U.S.C. § 103(a) as unpatentable over Yu '843 in view of Rao. (Examiner's answer, pages 6-7.)

II. Claim 5 under 35 U.S.C. § 103(a) as unpatentable over Yu '834 in view of Rao and Tang. (Id. at pages 7-8.)

III. Claim 7 under 35 U.S.C. § 103(a) as unpatentable over Yu '834 in view of Rao and Morimoto. (Id. at pages 8-9.)

IV. Claims 9 through 12 and 15 through 20 under 35 U.S.C. § 103(a) as unpatentable over Yu '534 in view of Rao. (Id. at pages 4-5.)

V. Claim 13 under 35 U.S.C. § 103(a) as unpatentable over Yu '534 in view of Rao and Tang. (Id. at pages 5-6.)

VI. Claim 14 under 35 U.S.C. § 103(a) as unpatentable over Yu '534 in view of Rao and Morimoto. (Id. at page 6.)

We reverse these rejections.

Under 35 U.S.C. § 103, the initial burden of establishing a prima facie case of obviousness rests on the examiner. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). In this case, it is our determination that the examiner has not met the initial burden of proof.

We first consider rejections I through III. Yu '843 teaches that "good local planarization [of a semiconductor wafer] can be readily achieved in a CMP process," but "obtaining a complete planarization with good uniformity on the scale of a wafer, or even a die, is not easy." (Column 2, lines 11-15.) To solve this problem, Yu '843 teaches a method in which, prior to the CMP process, a portion of the wafer surface is modified

in selected areas (e.g., areas that tend to be dished after the conventional CMP process) so that the polishing rate in these areas is altered (e.g., by modifying the area through a plasma nitridation process to create a material more resistant to polishing, thereby decreasing the polishing rate so that the dishing is eliminated). (Column 2, line 63 to column 3, line 4.) Alternatively, where large height differences exist in the surface to be planarized, Yu '843 teaches modifying the higher area through an ion implantation process to create a material less resistant to polishing, thereby increasing the polishing rate so that the overall surface is flat. (Column 3, lines 4-10.)

The examiner admits that Yu '843 does not teach the step of removing scratches formed on a dielectric layer during the CMP step, as recited in independent claim 1 on appeal. (Examiner's answer, page 7.) In an attempt to account for this difference, the examiner relies on the teachings of Rao. According to the examiner, Rao "teach[es] reflowing boron and phosphorus doped glass during integrated circuit chip manufacture...and teaches the benefits of the glass reflowing step." (Id.) The examiner then concludes that "[i]t would have been obvious to...reflow the glass of Yu..." and that "[o]ne of ordinary skill in this

art would have been motivated to make this substitution to the process of Yu et al. because of the teaching of Rao et al. that glass reflowing smooths [sic, smoothes] the profile of the glass and leads to higher production yields." (Id.)

The problem with the examiner's analysis, however, is that Yu '843 obtains a flat surface without the need for reflowing any dielectric layer. As we discussed above, Yu' 843 teaches that a flat surface is obtained by modifying the polishing rate of selected areas. Furthermore, Rao is directed to a method unrelated to a CMP process as described in Yu '843. Specifically, Rao describes controlling the profile of an interlevel dielectric prior to a reflowing step. (Column 2, lines 42-45.) According to Rao, the interlevel dielectric is deposited to a thickness significantly greater than needed, and then etched back to the desired thickness. (Column 2, lines 45-47.) The reflowing step in Rao is said to profile the contact hole sidewalls and smooth out the profile of the dielectric interlevel over a patterned stack 24 as shown in Figure 2.

Here, the examiner has not pointed to any disclosure in Rao even hinting that the reflowing step can be used in lieu of the process steps described in Yu '843 for the purpose of eliminating scratches following the CMP process, much less any

desirability or motivation for using such a reflowing step in Yu '843. It is only with the benefit of the appellants' own disclosure that the examiner has arrived at a conclusion of obviousness. In re Warner, 397 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967) ("[W]here the invention sought to be patented resides in a combination of old elements, the proper inquiry is whether bringing them together was obvious and not, whether one of ordinary skill, having the invention before him, would find it obvious through hindsight to construct the invention from elements of the prior art."); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("[T]he Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("[T]he best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.").

For these reasons, we cannot uphold rejection I.

The examiner has relied on Tang only for the teaching relating to a thermal anneal tool as recited in appealed claim

5, while Morimoto has been cited only for the teaching relating to steam ambients as recited in appealed claim 7. (Examiner's answer, page 8.) Since the examiner has not explained how Tang or Morimoto remedies the fundamental deficiencies of the rejection based on Yu '843 and Rao, it follows that we also cannot uphold rejections II and III.

Turning to rejections IV through VI, Yu '534 teaches a two-step process of plug (tungsten) formation using chemical mechanical planarization, in which the first CMP step is selective to the plug material and removes the upper layer of tungsten from an oxide surface while removing very little or no oxide from a wafer surface and the second CMP step is selective to the oxide and removes a portion of the insulation material to a level even with or slightly below the tungsten plugs. (Column 3, lines 27-57.)

The examiner admits that Yu '534, like Yu '843, does not teach the reflowing step recited in appealed claim 9. (Examiner's answer, page 5.) This difference notwithstanding, the examiner held that "[o]ne of ordinary skill in this art would have been motivated to" use Rao's reflowing step to carry out the process described in Yu '534.

We cannot agree for reasons analogous to those given above for rejections I through III. In particular, the examiner has not explained why one of ordinary skill in the art would have been led to use a reflowing step in Yu '534 when Yu '534 solves the problem of planarization using selective CMP steps. Moreover, Rao is concerned with smoothing the profile of the interlevel dielectric over a patterned stack following an etching step, as we discussed above. The examiner has not pointed to any disclosure, suggestion, or motivation in the prior art teachings that would have led one of ordinary skill in the art to combine the references in the manner as suggested by the examiner.

Under these circumstances, we also cannot uphold rejection IV.

As to rejections V and VI, the examiner has relied on Tang and Morimoto only for certain limitations recited in dependent claims 13 and 14. Since the examiner has not explained how these references overcome the fundamental deficiencies in the proposed combination of Yu '534 and Rao, we reverse rejections V and VI as well.

In summary, the examiner's 35 U.S.C. § 103(a) rejections of (i) claims 1 through 4, 6, and 8 as unpatentable over Yu '843 in

view of Rao, (ii) claim 5 as unpatentable over Yu '834 in view of Rao and Tang, (iii) claim 7 as unpatentable over Yu '834 in view of Rao and Morimoto, (iv) claims 9 through 12 and 15 through 20 as unpatentable over Yu '534 in view of Rao, (v) claim 13 as unpatentable over Yu '534 in view of Rao and Tang, and (vi) claim 14 as unpatentable over Yu '534 in view of Rao and Morimoto are reversed.

The decision of the examiner is reversed.

REVERSED

EDWARD C. KIMLIN Administrative Patent Judge	)	
PAUL LIEBERMAN Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ROMULO H. DELMENDO Administrative Patent Judge	)	

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