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BOARD OF PATENT APPEALS  
AND INTERFERENCES  
UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* MIKIHIRO KIMURA

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Appeal No. 93-4324  
Application 07/336,622<sup>1</sup>

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HEARD: NOVEMBER 18, 1994

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Before JERRY SMITH, HARKCOM, and FLEMING, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

*DECISION ON APPEAL*

This is a decision on appeal from the final rejection of claims 1, 10 and 12 through 24.

The invention is directed to a generic superlattice structure. Appellant's Figures 1 and 2 show the prior art superlattice structure in which the superlattice layers ((4b', 5b and 4b) shown in Figures 1 and (4c', 5c and 4c) shown in Figure 2) are formed by sequentially stacked layers on the surface of a semiconductor substrate. Appellant's invention is shown in

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<sup>1</sup> Application for patent filed April 10, 1989. According to appellant, the application is a continuation of Application 07/157,498, filed February 17, 1988, Abandoned.

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Figures 8 and 15. Figure 8 shows the superlattice layers formed by concave layers in a trench into the substrate. Figure 15 shows the superlattice layers formed by convex layers on a projection 30 of the substrate extending upwardly from the surface. Appellant's independent claims 10 and 12 are directed to the specific embodiment of Figure 15 and Appellant's independent claim 13 is directed to the embodiment of Figure 8. Appellant's independent claim 1 is directed to both embodiments of Figure 8 and Figure 15.

Claims 10 and 13 are reproduced as follows:

10. A superlattice semiconductor structure including a tunneling device comprising a semiconductor substrate having a major surface, an upstanding projecting region extending upwardly from the major surface of said semiconductor substrate, said upstanding projecting region having an upper top surface portion spaced from said major surface in a direction substantially normal thereto and a side surface portion extending substantially upwardly from the major surface to said upper top surface portion,

a superlattice structure having at least three thin superlattice layers formed on said top surface portion and on said side surface portion of said upstanding projecting region,

said at least three thin superlattice layers being sequentially stacked, each of said at least three superlattice layers having a different energy band structure and a thickness not greater than the de Broglie wavelength of an electron, and

a contact region for providing electrical contact to said superlattice structure, said contact region disposed on the major surface of said semiconductor substrate in a region other than said projecting region,

at least one superlattice layer of said projecting region extending onto the contact region,

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said projecting region including said tunneling device formed in said superlattice layers.

13. In a superlattice semiconductor structure including a tunneling device, an improvement for increasing flow of tunneling current comprising:

a semiconductor substrate having a major surface, a trench formed in the major surface of said semiconductor substrate, said trench having an end surface portion in a bottom of the trench spaced from said major surface in a direction normal thereto and a side surface portion extending between the major surface and the end surface portion, and

a superlattice structure having a plurality of superlattice layers formed in said trench at least along the end surface portion and the side surface portion of said trench,

said superlattice structure including said tunneling device therein, said tunneling device having:

a first of said superlattice layers of a first conductivity type and having a first contact connected thereto, and a second of said superlattice layers of a second conductivity type opposite to said first conductivity type having a second contact connected thereto,

said first and second layers separated by a plurality of thin superlattice layers alternating between a first semiconductor composition and a second semiconductor composition to produce a plurality of stepped variations in an energy band structure thereof;

said thin superlattice layers being sequentially stacked, each of said thin superlattice layers having a different energy band structure and a thickness not greater than the de Broglie wavelength of an electron, and

a contact region for providing electrical contact to said superlattice structure, said contact region disposed on the major surface of the semiconductor substrate in a region other than said trench region,

at least one of said superlattice layers extending from said trench onto said contact region for making contact with another device,

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said element including said tunneling device formed in said superlattice layers.

The Examiner relies on the following references:

Baglee et al. (Baglee) 4,721,987 Jan. 26, 1988

Kapon et al. (Kapon), "Molecular beam epitaxy of GaAs/AlGaAs superlattice heterostructures on nonplanar substrates," *Appl. Phys. Lett.*, 50(6), pp. 347-349 (Feb. 1987).

Claims 1, 10 and 12 through 24 stand rejected under 35 U.S.C. § 103 as unpatentable over the Appellant's admitted prior art shown in Figures 1 through 7B in view of Baglee and Kapon.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs and answers for the respective details thereof.

#### OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 1, 10 and 12 through 24 are directed to subject matter that would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103 as evidenced by the Appellant's admitted prior art shown in Figures 1 through 7B in view of Baglee and Kapon.

At the outset, we note that Appellant has indicated that claims 1, 10 and 12 through 24 do not stand or fall together. However, Appellant has only argued the independent claims 1, 10, 12 and 13 and has not argued the particulars of the dependent

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claims. Since the patentability of the dependent claims was not argued separately, our reviewing court has ruled that they stand or fall with the independent claims. *In re Sernaker*, 702 F.2d 989, 991, 217 USPQ 1, 3, (Fed. Cir. 1983). Also, see *In re Nielson*, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987); *In re Kaslow*, 707 F.2d 1366, 217 USPQ 1089 (Fed. Cir. 1983); *In re Wiseman*, 596 F.2d 1019, 201 USPQ 658 (CCPA 1979). Since the patentability of the Appellant's dependent claims is not argued separately, we find that they stand or fall with the independent claims.

Appellant argues that a *prima facie* case has not been established because the Examiner's rejection does not show the structure of Appellant's Figures 10-12 wherein the superlattice layers extend to the contact region as correspondingly described in Appellant's specification on pages 16 through 20. Appellant further submits "that superlattice layers which cover both the side walls and the stepped portion, whether in a trench or in a projection, and which extend to a contact region as illustrated in Figure 11B for example, are clearly missing from Baglee and Kapon" (brief, page 10).

Appellant's claim 1 sets forth the above limitation as the following:

a contact region for providing electrical contact to at least one layer of said superlattice structure, said contact region disposed on the major surface of

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the semiconductor substrate in a region other than said stepped surface portion of said element,

said at least one layer of said superlattice structure extending onto the contact region for making electrical contact....<sup>2</sup>

Appellant's independent claims 10, 12 and 13 similarly set forth the above limitation of extending at least one layer of the superlattice layer onto the contact region from either a trench or projection.

However, extending semiconductor layers on a semiconductor substrate to form an integrated circuit is the basic concept of an integrated circuit. Baglee discloses in Figures 1 and 2 a trench 11 in which semiconductor layers are extended onto a contact region (the region on either side of the trench 11) for making electrical contact with another device (transistor 10). Therefore, we find that it would have been obvious to one of ordinary skill in the art to extend at least one of semiconductor superlattice layers of Kapon onto a contact region for making electrical contact with another device as taught by Baglee to obtain the Appellant's claimed limitation.

Appellant further argues that there is no basis "for combining Kapon et al. with the admitted prior art of Figure 1, both because the admitted prior art shows a *projecting*

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<sup>2</sup>Claim 1 properly on appeal appears in Amendment F, Paper No. 16, filed January 22, 1992. The claim in the brief is incorrect.

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superlattice (rather than the *grooved* structure of Kapon) and because the objects of the admitted art and those of Kapon are nowhere identified as being the same" (brief, page 12).

Appellant states that Kapon's object is to utilize the growth features of the structure in order to achieve controllable patterning.

However, we find that Kapon does disclose that the object is to provide improved superlattice structures such as the Appellant's admitted prior art. Kapon discusses on page 347 in the abstract the feasibility of utilizing superlattice heterostructures on non-planar substrates. Kapon's Figure 1 shows a cross section of a superlattice layer in a groove and Kapon's Figure 3(c) shows a possible way to realize a well structure, by growing a quantum well heterostructure in a groove. Finally, Kapon summarizes in the final paragraph that they have grown superlattice heterostructures on non-planar substrates that provide suitable physical properties and can achieve lateral potential barriers in quantum well heterostructures in order to obtain semiconductors with reduced carrier dimensionality. Clearly, Kapon teaches that suitable superlattice semiconductor structures can be provided by using non-planar substrates in order to take up less surface area of a semiconductor chip. From the Kapon disclosure, it is clear the objective is to provide superlattice semiconductor structures formed on non-planar

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substrate surfaces such as a trench or a groove and it was this teaching that the Examiner is relying upon in the rejection.

In addition, the Examiner is not relying on the admitted prior art of Figure 1 for showing a projecting superlattice (rather than the *grooved* structure of Kapon). The Examiner asserts that it would have been obvious to modify the admitted prior art of Figure 1 which shows a planar structure into a trench structure as shown in Kapon and Baglee.

The basis of combining prior art references is as follows:  
"[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783, 1784 (Fed. Cir. 1992), *citing In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Kapon teaches that surface area of the substrate wafer surface may be saved by providing a superlattice semiconductor structure in a trench or groove. In addition, Baglee teaches that the surface area of the substrate wafer may be saved by utilizing a trench etched in the substrate in which semiconductor layers placed in column 1, lines 35-37. On page 9 of the specification, Appellant discloses that his invention of utilizing either a trench or convex structures is used to decrease the surface area of substrate that would be utilized by the prior art planar layers shown in Appellant's

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Figures 1 and 2. Thus, Baglee and Kapon teach the same reason for providing a trench structure and that it is desirable to utilize non-planar layers formed in a trench in the substrate in order to save the surface area of the substrate. Therefore, we find that Baglee and Kapon both provide the desirability of modifying the admitted prior art planar layers into non-planar layers formed in a trench etched in the substrate.

Finally, Appellant argues that Baglee and Kapon fail to specifically teach a convex region of the substrate as set forth in claims 1, 10 and 12. Appellant discloses the projection structure in Figure 15 and on page 27, lines 1-22. Appellant discloses on page 9 that the purpose of the projection structure as well as the trench structure is to provide more area for the superlattice layers by utilizing the side wall portion without having to provide more substrate surface area.

We note that not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. See *In re Preda*, 401 F.2d 825, 159 USPQ 342 (CCPA 1968); *In re Shepard*, 319 F.2d 194, 138 USPQ 148 (CCPA 1963); and *In re Sernaker*, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). Skill in the art is presumed. See *In re Sovish*, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985).

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As shown above, both Baglee and Kapon teach that a trench structure provides more area for semiconductor layers and saves valuable substrate surface area. By analogy, this is the same solution employed in densely populated cities where land area is limited. In these situations, designers have provided more floor area by either building projecting structures above the land (upper floors of high building) or building trench structures below the land (basement floors of buildings) in order to provide more density using the same land area. Both Baglee and Kapon teach that one can gain more semiconductor layer area by forming layers in a trench etched in the substrate. One of ordinary skill in the art from this teaching would also recognize the inverse of the Baglee and Kapon trench is a projection structure and provides the same function. Therefore, Baglee and Kapon provide reasonable inferences which the artisan would have logically drawn therefrom to obtain the Appellant's convex structure as claimed.

In view of the foregoing, the decision of the Examiner rejecting claims 1, 10 and 12 through 24 under 35 U.S.C. § 103 is affirmed. Accordingly, the decision of the Examiner is affirmed.

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No time period for taking any subsequent action in  
connection with this appeal may be extended under 37 CFR  
1.136(a).

AFFIRMED

*Jerry Smith*

JERRY SMITH )  
Administrative Patent Judge)

*Gary V. Harkcom*

GARY V. HARKCOM )  
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*Michael R. Fleming*

MICHAEL R. FLEMING )  
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